Notice of Allowability	Application No.	Applicant(s)	
	10/797,753	HE ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/03/2006*.

2. ☒ The allowed claim(s) is/are *1-3,5-12 and 14-19*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

Response to Amendment

1. Amendment filed on 04/03/2006 has been entered.

In response to the Office Action dated 01/24/2006, Applicants has amended claims 1-3 and 5-8.

Claim 4 has been cancelled.

Claims 1-3 and 5-21 are now pending in the application.

Examiner's Amendment

3.1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3.2. Authorization for this examiner's amendment was given in a telephone interview with J.J. Namiki (Reg. No. 51148) on May 25, 2006.

3.2.1. Claim 9. (Currently Amended): An assembly comprising: an apparatus comprising: a signal layer including a first and second signal trace located along a first plane, each of the first and second signal traces comprises a first segment with a first segment width, and a second segment with a second segment width;

a [first] reference [plane] layer located along a second plane that is substantially parallel with the first plane coupled to the first and the second signal trace, the reference layer includes[ing] a [first] slot substantially parallel to the first and second signal traces, the slot comprising a first portion and a second portion having a first portion width and a second portion width, respectively; and wherein the first and second

portions of the slot correspond to the first and second segments, respectively, of the first and second signal traces.

[a dielectric layer having at least a first portion disposed between the signal layer and the first reference plane;] a processor coupled to the apparatus; and a networking interface coupled to the apparatus.

3.2.2. Claim 10. (Currently Amended): The assembly of claim 9 wherein the first and second signal traces are coupled to the processor and a [the] memory device.

3.2.3. Claim 11. (Currently Amended): The assembly of claim 9, further comprising a dielectric layer that is at least partially disposed between the signal layer and the reference layer [wherein each of the first and second signal traces comprise a first portion with a first width and a second portion with a second width].

3.2.4. Claim 12. (Currently Amended): The assembly of claim [11] 9 wherein spacing between the first and the second signal trace remains substantially constant in both the first and second segments [the first slot comprises a first portion and a second portion having a first slot width and a second slot width, respectively].

3.2.5. Claim 13. (Cancelled)

3.2.6. Claim 14. (Currently Amended): The assembly of claim [9] 11 further comprising: another [a second] reference layer located along a third plane that is substantially parallel with the first plane, coupled to the first and the second signal trace, the other reference layer [plane] including [a second] another slot substantially parallel to the first and second signal traces; and the dielectric layer is further [includes a second portion] partially disposed between the signal layer and the other [second] reference layer [plane].

3.2.7. Claim 16. (Currently Amended): A system comprising: an assembly comprising: an apparatus comprising: a signal layer including a first and second signal trace; located along a first plane, each of the first and second signal traces comprises a first segment with a first segment width, and a second segment with a second segment width; a [first] reference layer [plane] located along a second plane that is substantially parallel with the first plane coupled to the first and the second signal trace, the reference layer includes[ing] a [first] slot substantially parallel to the first and second signal traces, the slot comprising a first portion and a second portion having a first portion width and a second portion width, respectively; and wherein the first and second portions of the slot correspond to the first and second segments, respectively, of the first and second signal traces [a dielectric layer having at least a first portion disposed between the signal layer and the first reference plane]; and a processor coupled to the apparatus; and a networking device coupled to the assembly.

3.2.8. Claim 18. (Currently Amended): The system of claim 16 wherein the assembly further comprises an interface to a persistent storage and wherein the system further comprises the persistent storage coupled to the interface to the persistent storage.

3.2.9. Claim 19. (Currently Amended): A method of routing circuit board traces comprising: routing a first signal trace and a second signal trace [substantially parallel to the first signal trace on a signal] along a first plane of a circuit board, each of the first and second signal traces comprises a first segment with a first segment width, and a second segment with a second segment width; and routing a slot in a reference layer located along a second plane of the circuit board that is substantially parallel with the first plane coupled to the first and the second signal trace, the slot is substantially parallel to the first and the second signal traces the slot comprising a first portion and a second portion having a first portion width and a second portion width, respectively [for at least a portion of the first and second signal traces]; and wherein the first and second portions of the slot correspond to the first and second segments, respectively, of the first and second signal traces.

3.2.10. Claim 20. (Cancelled)

3.2.11. Claim 21. (Cancelled)

Allowed Claims

4.1. Claims 1-3, 5-12 and 14-19 are allowed.

4.2. The following is a statement of reasons for the indication of allowance:

Carey teaches a reference plane includes slot substantially parallel to the first and second signal traces, however such slot in the same plane but Applicant teaches the slot in different reference plane. Itoh teaches a reference plane including a slit-shaped through holes but such holes comes though all layers and substantially parallel to just one signal trace (not to pair of signal traces) and filled with solders. Pinney discloses each of the first A and second C signal traces comprise a first portion with a first width, and a second portion with a second width, except Pinney does not teach a reference plane includes the slot.

Limitation "a reference layer located along a second plane that is substantially parallel with the first plane coupled to the first and the second signal trace, the reference layer includes a first slot substantially parallel to the first and second signal traces" in combination with other claimed limitations in independent claims 1 are not disclosed or suggested by the prior art.

4.3. Rejoining and allowing claims 9-12 and 14-19.

Claims 9-12 and 14-19 withdrawn from consideration pursuit to the restriction requirement, have been amended to include all of the allowable combinations and have been rejoined because they contain similar allowed subject matter to the elected claims as explained in the reason for allowance.

5.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

5.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

5.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

RANDY W. GIBSON
PRIMARY EXAMINER